

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: Not yet assigned
Filing Date: Herewith
Applicant: Toshiya Yokogawa et al.
Group Art Unit: Not yet assigned
Examiner: Not yet assigned
Title: Equipment for Communication System and
Semiconductor Integrated Circuit Device
Attorney Docket: 5077-000075/DVA

Director of the United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant hereby submits an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS, AND OTHER INFORMATION

The patents, publications and other information submitted for consideration by the Office (except unpublished U.S. patent applications) are listed on Form 1449 attached hereto.

II. COPIES

A. ___ Submitted herewith is a legible copy of (i) each U.S. patent application publication and U.S. and foreign patent; (ii) each publication or that portion which caused it to be listed; (iii) for each cited pending U.S. application, the application specification including the claims, and any drawing of the application which caused it to be listed including the claims directed to that portion; and (iv) all other information or that portion which caused it to be listed.

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APPLICANT

Toshiya Yokogawa et al.

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GROUP

U.S. PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
1.		6,483,100	11/2002	Williams et al.		
2.		5,091,759	02/1992	Shih et al.		
3.		5,284,782	02/1994	Jeong et al.		
4.		5,463,978	11/1995	Larkin et al.		
5.		5,492,857	02/1996	Reedy et al.		
6.		6,057,566	02/2000	Eisenbeiser et al.		
7.		5,013,685	05/1991	Chiu et al.		
8.		5,324,682	06/1994	Tserng		
9.		6,025,613	02/2000	Bito et al.		
10.		6,258,616	06/2001	Cunningham et al.		
11.		5,488,237	01/1996	Kuwata		
12.		6,380,569	04/2002	Chang et al.		

FOREIGN PATENT DOCUMENTS

Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation Yes	No
1.		05013446 A	01/22/1993	Japan		Partial	
2.		0 555 886 A2	08/18/1993	Europe			

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EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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FILING DATE

GROUP

OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)

Ref. Desig.	Examiner's Initials	
1.		Wen-Chau Liu et al.; "Application of δ -doped Wide-Gap Collector Structure for High-Breakdown and Low-Offset voltage Transistors"; American Institute of Physics; September 7, 1998.
2.		Asen Asenov et al.; "Suppression of Random Dopant-Induced Threshold Voltage Fluctuations in Sub-0.1- μ m MOSFET's with Epitaxial and δ -Doped Channels"; IEEE Transaction on Electron Devices; Vol. 46, No. 8; August 1999.
3.		Hata (US patent Application Publication 2002/0008242 A) US class 257/79

Examiner:

Date Considered:

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.